

What is Claimed Is:

1. A graphics processing unit, comprising:
a clock generator configured to generate a clock signal; and
a controller coupled to the clock generator, wherein the controller is configured to receive the clock signal, compare the clock signal with a synchronization signal to generate a timing signal, and transmit the timing signal to a second graphics processing unit.
2. The graphics processing unit of claim 1, wherein the graphics processing unit is configured to generate a first portion of an image and the second graphics processing unit is configured to generate a second portion of the image such that the first portion and the second portion synchronously form the image.
3. The graphics processing unit of claim 1, wherein the controller is further configured to transmit the timing signal to the graphics processing unit.
4. The graphics processing unit of claim 1, wherein the controller is configured to transmit the timing signal to the graphics processing unit and the second graphics unit in response to the clock signal and the synchronization signal being in phase.
5. The graphics processing unit of claim 1, wherein the synchronization signal is an external synchronization signal.
6. The graphics processing unit of claim 1, wherein the controller is further configured to transmit a stereo field signal to the second graphics processing unit.
7. The graphics processing unit of claim 1, further comprising:
a frame buffer having a front portion and a back portion; and
a swap ready input/output element through which a swap ready signal is communicated to the second graphics processing unit, wherein the swap ready signal indicates to the second graphics processing unit that an image content stored in the back portion of the frame buffer is ready to be transferred to the front portion of the frame buffer.

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8. The graphics processing unit of claim 7, wherein the frame buffer is configured to generate the swap ready signal in response to a completed transfer of the image content from the back portion to the front portion.
9. The graphics processing unit of claim 7, wherein the frame buffer is configured to generate the swap ready signal in response to a soon to be completed transfer of the image content from the back portion to the front portion.
10. The graphics processing unit of claim 1, wherein the controller is further configured to supply a vertical timing reset signal to the graphics processing unit.
11. The graphics processing unit of claim 1, wherein the controller is further configured to supply a horizontal timing reset signal to the graphics processing unit.
12. The graphics processing unit of claim 1, further comprising a vertical timing reset signal counter configured to keep track of the number of vertical timing reset signals for use in deriving a frame count.
13. The graphics processing unit of claim 12, wherein the controller is further configured to provide the frame count to the second graphics processing unit.
14. A graphics processing unit, comprising:
 - means for generating a clock signal; and
 - means for receiving the clock signal, comparing the clock signal with a synchronization signal to generate a timing signal, and transmitting the timing signal to a second graphics processing unit.
15. The graphics processing unit of claim 14, wherein the graphics processing unit is configured to generate a first portion of an image and the second graphics processing unit is configured to generate a second portion of the image such that the first portion and the second portion synchronously form the image.
16. The graphics processing unit of claim 14, wherein the synchronization signal is an external synchronization signal.

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17. The graphics processing unit of claim 14, further comprising means for transmitting a stereo field signal to the second graphics processing unit.
18. The graphics processing unit of claim 14, further comprising:
 - means for buffering an image content; and
 - means for providing a swap ready signal to the second graphics processing unit to indicate to the second graphics processing unit that the image content is ready to be transferred from a back portion to a front portion of the buffering means.
19. The graphics processing unit of claim 14, further comprising means for keeping track of the number of vertical timing reset signals for use in deriving a frame count.
20. The graphics processing unit of claim 19, further comprising means for sending the frame count to the second graphics processing unit.
21. A graphics module, comprising:
 - a first graphics processing unit having:
 - a clock generator configured to generate a clock signal;
 - a controller coupled to the clock generator, wherein the controller is configured to receive the clock signal, compare the clock signal with a synchronization signal to generate a timing signal, and transmit the timing signal; and
 - a second graphics processing unit coupled to the first graphics processing unit, wherein the second graphics processing unit is configured to receive the timing signal from the first graphics processing unit.
22. The graphics module of claim 21, wherein the first graphics processing unit is configured to display a first portion of an image and the second graphics unit is configured to display a second portion of the image, wherein the first portion and the second portion synchronously form the image.

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23. The graphics module of claim 21, wherein the controller is further configured to transmit a stereo field signal from the first graphics processing unit to the second graphics processing unit.

24. The graphics module of claim 21, wherein the first graphics processing unit further comprises:

a frame buffer having a front portion and a back portion; and

a first swap ready input/output element configured to transmit a swap ready signal to the second graphics processing unit, wherein the swap ready signal indicates whether an image content stored in the back portion of the frame buffer is ready to be transferred to the front portion of the frame buffer.

25. The graphics module of claim 21, wherein the graphics module is implemented on a silicon substrate.